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10/575,819	04/13/2006	Seong-Young Lee	AB-1867 US	5258
32605 7590 11/26/2008 MACPHERSON KWOK CHEN & HEID LLP			EXAMINER	
2033 GATEWAY PLACE SUITE 400 SAN JOSE, CA 95110			SALERNO, SARAH KATE	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

	Application No.	Applicant(s)
	10/575,819	LEE ET AL.
Office Action Summary	Examiner	Art Unit
	SARAH K. SALERNO	2814
The MAILING DATE of this communication ap Period for Reply	ppears on the cover sheet with the	correspondence address
A SHORTENED STATUTORY PERIOD FOR REPLEWHICHEVER IS LONGER, FROM THE MAILING DEVELOPMENT OF THE MAILING	DATE OF THIS COMMUNICATIO .136(a). In no event, however, may a reply be tind d will apply and will expire SIX (6) MONTHS from te, cause the application to become ABANDONE	N. mely filed the mailing date of this communication. ED (35 U.S.C. § 133).
Status		
Responsive to communication(s) filed on <u>04 S</u> This action is <b>FINAL</b> . 2b) ☑ This action for allowed closed in accordance with the practice under	is action is non-final. ance except for formal matters, pr	
Disposition of Claims		
4)  Claim(s) 1-14,16-22 and 24-26 is/are pending 4a) Of the above claim(s) is/are withdra 5)  Claim(s) is/are allowed.  6)  Claim(s) 1-14,16-22 and 24-26 is/are rejected 7)  Claim(s) is/are objected to.  8)  Claim(s) are subject to restriction and/s	awn from consideration.	
Application Papers		
9) The specification is objected to by the Examin 10) The drawing(s) filed on is/are: a) ac Applicant may not request that any objection to the Replacement drawing sheet(s) including the correct 11) The oath or declaration is objected to by the E	cepted or b) objected to by the edrawing(s) be held in abeyance. Section is required if the drawing(s) is ob	e 37 CFR 1.85(a). ejected to. See 37 CFR 1.121(d).
Priority under 35 U.S.C. § 119		
12) Acknowledgment is made of a claim for foreig a) All b) Some * c) None of:  1. Certified copies of the priority document 2. Certified copies of the priority document 3. Copies of the certified copies of the priority document application from the International Bureat * See the attached detailed Office action for a list	nts have been received. nts have been received in Applicat ority documents have been receiv au (PCT Rule 17.2(a)).	ion No ed in this National Stage
Attachment(s)  1) Notice of References Cited (PTO-892)  2) Notice of Draftsperson's Patent Drawing Review (PTO-948)  3) Information Disclosure Statement(s) (PTO/SB/08)  Paper No(s)/Mail Date	4)  Interview Summary Paper No(s)/Mail D 5)  Notice of Informal I 6)  Other:	ate

Art Unit: 2814

#### **DETAILED ACTION**

### Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 09/04/08 has been entered.

## Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

- (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.
- 3. Claims 1-4, 6-8 and 26 are rejected under 35 U.S.C. 102(e) as being anticipated by Hong et al. (US PGPub 2004/0066481).
  - Claim 1: Hong teaches a thin film transistor comprising (FIG. 4E):

a gate electrode (201a); a gate insulating layer (208) formed on the gate electrode; a semiconductor layer (205) formed on the gate insulating layer and disposed opposite the gate electrode; a source electrode (202a) and a drain electrode (202b) that are formed at least in part on the semiconductor layer and face each other:

a passivation layer formed on the source electrode, the drain electrode, and a portion of the semiconductor layer that is not covered with the source electrode and the drain electrode [0050]; and

Page 3

a shielding electrode (224) formed on the passivation layer and disposed on a region between the source electrode and the drain electrode, wherein the shielding electrode provides voltage shielding fro the region on which it is disposed, and wherein the shielding electrode comprises a transparent electrode (FIG. 4a-e; [0047-0051]).

Claim 2: Hong teaches the shielding electrode is electrically isolated (FIG. 4a-e; [0047-0051]).

Claim 3: Hong teaches a shielding electrode is supplied with a predetermined voltage to prevent the accumulation of electric charge on the light-shield film (FIG. 4a-e; [0047-0051]).

Claim 4: Hong teaches the predetermined voltage supplied to the shielding electrode is equal to or lower than a ground voltage (FIG. 4a-e; [0047-0051]).

Claim 6: Hong teaches the shielding electrode comprises IZO or ITO (FIG. 4a-e; [0047-0051]).

Claim 7: Hong teaches the shielding electrode has a shape of horseshoes (FIG. 4a-e; [0047-0051]).

Claim 8: Hong teaches the passivation layer comprises an organic insulator (FIG. 4a-e; [0047-0051]).

Claim 26: Hong teaches the shielding electrode is formed on the channel portion of the thing film transistor (FIG. 4a-e; [0047-0051]).

## Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hong et al. (US PGPub 2004/0066481), as applied to claim 3 above, and further in view of Kubota (JP Pub No. 10-098190 of record)

Regarding claim 5, as described above, Hong substantially read on the invention as claimed, except Hong does not teach teaches the predetermined voltage supplied to the shielding electrode is a negative voltage. Kubota teaches the predetermined voltage supplied to the shielding electrode is a negative voltage [0039] to prevent characteristic degradation of the image display device (Abs). Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the voltage supplied to the shielding electrode to be negative to prevent characteristic degradation as taught by Kubota (Abs, [0039]).

6. Claims 9-12, and 18-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hong et al. (US PGPub 2004/0066481) in view of Nishida et al. (US PGPub 2002/0159016).

Claim 9: Hong teaches a thin film transistor array panel comprising: a gate line and a data tie line;

a first thin film transistor including a control electrode, an input electrode, an output electrode, and a channel portion disposed between the input electrode and the output electrode and generating a gate signal to be applied to the gate line;

Page 5

a second thin film transistor including a gate electrode connected to the gate line, a source electrode connected to the data line, a drain electrode, and a channel portion disposed between the source electrode and the drain electrode and transmitting a data signal from the data line in response to the gate signal from the gate line;

a pixel electrode connected to the drain electrode to receive the data signal; and a first shielding electrode disposed on the channel portion of the first thin film transistor (FIG. 4a-e; [0047-0051]).

Hong does not teach the first shielding electrode is formed of the same layer as the pixel electrode. Nishida teaches the first shielding electrode (26) is formed of the same layer as the pixel electrode (27) to decrease the number of processing steps (FIG. 2; [0318]). Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the device taught by Hong to have the first shielding electrode formed on the same layer as the pixel electrode to decrease the number of processing steps as taught by Nishida (FIG. 2; [0318]).

Claim 10: Hong teaches the shielding electrode is electrically isolated (FIG. 4a-e; [0047-0051]).

Claim 11: Hong teaches a shielding electrode is supplied with a predetermined voltage to prevent the accumulation of electric charge on the light-shield film (FIG. 4a-e; [0047-0051]).

Claim 12: Hong teaches the predetermined voltage supplied to the shielding electrode is equal to or lower than a ground voltage (FIG. 4a-e; [0047-0051]).

Claim 18: Hong teaches the passivation layer comprises an organic insulator (FIG. 4a-e; [0047-0051]).

Claim 19: Hong teaches a display device comprising:

a gate line and a data line; a first thin film transistor including a channel portion and generating a gate signal to be applied to the gate line; a second thin film transistor transmitting a data signal from the data line in response to the gate signal from the gate line;

a pixel electrode connected to the second thin film transistor to receive the data signal; a shielding electrode disposed on the channel portion of the first thin film transistor; and a common electrode facing the pixel electrode (FIG. 4a-e; [0047-0051]).

Hong does not teach wherein the shielding electrode is formed of the same layer as the pixel electrode. Nishida teaches the first shielding electrode (26) is formed of the same layer as the pixel electrode (27) to decrease the number of processing steps (FIG. 2; [0318]). Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the device taught by Hong to have the first shielding electrode formed on the same layer as the pixel electrode to decrease the number of processing steps as taught by Nishida (FIG. 2; [0318]).

Claim 20: Hong teaches the shielding electrode faces, the common electrode (FIG. 12).

Art Unit: 2814

7. Claims 13-14 and 21-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hong et al. (US PGPub 2004/0066481) in view of Nishida et al. (US PGPub 2002/0159016) as applied to claim 11 above, and further in view of Kubota (JP Pub No. 10-098190 of record)

Regarding claim 13, as described above, Hong substantially read on the invention as claimed, except Hong does not teach teaches the predetermined voltage supplied to the shielding electrode is a negative voltage. Kubota teaches the predetermined voltage supplied to the shielding electrode is a negative voltage [0039] to prevent characteristic degradation of the image display device (Abs). Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the voltage supplied to the shielding electrode to be negative to prevent characteristic degradation as taught by Kubota (Abs, [0039]).

Claim 21: Kubota teaches the shielding electrode is supplied with a predetermined voltage lower than a voltage applied to the common electrode [0004, 0013, 0018-0019, 0022, 0050-0059].

Claims 14 & 22: Kubota teaches the predetermined voltage supplied to the first shielding electrode has a magnitude for turning of the second thin film transistor [0004, 0013, 0018-0019, 0022, 0050-0059].

8. Claims 16-17 and 24-25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hong et al. (US PGPub 2004/0066481) in view of Nishida et al. (US

PGPub 2002/0159016) as applied to claim 9 above, and further in view of Kubo (US Patent 6,091,467 of record)

Regarding claim 16, as described above, Hong and Nishida substantially read on the invention as claimed, except Hong and Nishida do not teach a second shielding electrode disposed on the channel portions of the second thin film transistor and including the same layer as the pixel electrode. Kubo teaches a second shielding electrode disposed on the channel portions of the second thin film transistor and including the same layer as the pixel electrode (Description of the Related Art; Figs. 9-10, 12) as being known in the art. Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the device taught by Hong and Nishida to have a second shielding electrode disposed on the channel portions of the second thin film transistor and including the same layer as the pixel electrode as taught by Kubo to be known in the art (Description of the Related Art; Figs. 9-10, 12)

Claim 17: Kubo teaches an insulating layer disposed between the first and the second thin film transistors and the first and the second shielding electrodes (Description of the Related Art; Figs. 9-10, 12).

Claim 24: Kubo teaches a dielectric layer (216) disposed between the shielding electrode and the common electrode (FIG. 12).

Claim 25: Kubo teaches the dielectric layer (216) comprises a liquid crystal layer (col. 2 lines 10-20).

Art Unit: 2814

# Response to Arguments

9. Applicant's arguments with respect to claims 1-14, 16-22 and 24-26 have been considered but are moot in view of the new ground(s) of rejection.

Art Unit: 2814

#### Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to SARAH K. SALERNO whose telephone number is (571)270-1266. The examiner can normally be reached on M-F 8:00-4:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on (571) 272-1705. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/S. K. S./ Examiner, Art Unit 2814

/Theresa T. Doan/ Primary Examiner, Art Unit 2814